WHAT IS CLAIMED IS:

1. A MMIC-based E-Band transceiver front-end comprising:

a first MMIC device comprising,

a transmission circuit for receiving a data stream input at a baseband frequency, mixing the data stream with an LO signal having an E-Band frequency, and transmitting a resultant data stream at an upconverted E-Band frequency;

a receiver circuit for receiving a data stream having an E-Band frequency, mixing the received data stream with an LO signal having an E-Band frequency, and downconverting the resultant mixed received signal to an intermediate frequency (IF); and

an LO signal circuit for dividing a received LO signal at an E-Band frequency and communicating the LO signal to said transmission and receiver circuits;

a second MMIC device comprising a multiplier circuit for receiving an LO signal at a reference frequency, and multiplying the LO signal to an E-Band frequency;

a third MMIC device comprising,

a second downconversion circuit for mixing the mixed received IF signal with an LO signal, and downconverting the resultant mixed received signal to a baseband frequency, and

an LO generation circuit for generating an LO signal, communicating the LO signal to said second MMIC device, coupling the LO signal, dividing the coupled LO signal, and communicating the divided LO signal to the second downconversion circuit.

2. The E-Band transceiver front-end according to Claim 1, wherein said first, second, and third MMIC devices are manufactured by a p-HEMT process.

3. The E-Band transceiver front-end to Claim 1, wherein said first and second MMIC devices are manufactured by a p-HEMT process and said third MMIC device is manufactured by a MESFET process.

4. The E-Band transceiver front-end according to Claim 1, wherein said transceiver front-end transmits and receives over three frequency ranges including 71-76 GHz, 81-86 GHz and 92-95 GHz.

5. The E-Band transceiver front-end according to Claim 2, wherein said transceiver front-end transmits and receives over four 1.25 GHz channels within each of the 71-76 GHz , 81-86 GHz, and 92-95 frequency ranges.

6. The E-Band transceiver front-end according to Claim 1, wherein said MMIC devices are gallium arsenide (GaAs) devices.

7. The E-Band transceiver front-end according to Claim 1, wherein said transceiver front-end is adapted to communicate with another transceiver front-end in a full-duplex scheme.

8. The E-Band transceiver front-end according to Claim 1, wherein said transmission circuit includes a fundamental mixer and at least one amplifier downstream of said mixer.

9. The E-Band transceiver front-end according to Claim 1, wherein said receiving circuit includes a low noise amplifier, a bandpass filter downstream said low noise amplifier, and a fundamental mixer downstream said low noise amplifier.

10. The E-Band transceiver front-end according to Claim 1, wherein said LO signal circuit comprises a power divider and at least one amplifier downstream each output of said divider.

11. The E-Band transceiver front-end according to Claim 1, wherein said multiplier circuit comprises an X2 multiplier, a first bandpass filter downstream said X2 multiplier, a circuit amplifier downstream said first bandpass filter, a X4 multiplier downstream of said multiplier circuit amplifier, and a multiplier circuit bandpass filter downstream of said X4 multiplier.

12. The E-Band transceiver front-end according to Claim 1, said second downconversion circuit comprises at least one amplifier, a low pass filter downstream of said at least one amplifier, and a mixer downstream of said low pass filter.

13. The E-Band transceiver front-end according to Claim 1, wherein said LO generation circuit comprises an oscillator, at least one buffering amplifier downstream said oscillator, a coupler between said oscillator and said at least one buffering amplifier, a power divider downstream of said coupler, and a second amplifier downstream an output of said power divider.

14. The E-Band transceiver front-end according to Claim 1, wherein a sub-harmonic mixing scheme is utilized.

15. The E-Band transceiver front-end according to Claim 14, said wherein said transmission circuit and said receiver circuit each utilize singly balanced sub-harmonic mixers.

16. The E-Band transceiver front-end according to Claim 15, wherein said multiplier circuit comprises a circuit amplifier, a X4 multiplier downstream of said multiplier circuit amplifier, and a multiplier circuit bandpass filter downstream of said X4 multiplier.

17. A MMIC-based E-Band transceiver front-end comprising:

a first MMIC device comprising,

a transmission circuit comprising a fundamental transmission mixer, at least one transmission amplifier downstream said transmission mixer, wherein a data steam is input into said transmission mixer, and wherein an output from said at least one amplifier is transmitted;

a receiver circuit comprising a low noise amplifier, a receiver bandpass filter downstream said low noise amplifier, and a fundamental receiver mixer, wherein a received signal is communicated to an input of said low noise amplifier, and wherein an output of said receiver mixer is communicated to a third MMIC device; and

an LO signal circuit comprising a power divider, a transmission LO amplifier in communication with a first output of said power divider, and a receiver LO amplifier in communication with a second output of said power divider, wherein an output of said transmission LO amplifier is communicated to an input of said transmission mixer, and an output of said receiver LO amplifier is communicated to an input of said receiver mixer;

a second MMIC device comprising a multiplier circuit comprising an X2 multiplier, a first multiplier circuit bandpass filter downstream of said X2 multiplier, a multiplier circuit amplifier downstream of said first multiplier circuit bandpass filter, a X4 multiplier downstream of multiplier circuit amplifier, and a second multiplier circuit bandpass filter downstream of said X4 multiplier, wherein an output of said X4 multiplier is communicated to an input of said power divider of said first MMIC device;

said third MMIC device comprising,

an IF circuit comprising an IF amplifier, a low pass filter downstream of said IF amplifier, and a baseband mixer downstream of said low pass filter, wherein an output of said receiver mixer from said first MMIC device is communicated to an input of said IF amplifier, and wherein said baseband mixer provides an output data stream; and

an LO generation circuit comprising a fixed tuned oscillator, a first buffering amplifier downstream of said fixed tuned oscillator, a coupler between said fixed tuned oscillator and said first buffering amplifier, a third MMIC device power divider downstream of said coupler, and a second buffering amplifier downstream of a first output of said third MMIC device power divider, wherein an output from said first buffering amplifier is communicated to an input of said X2 multiplier of said second MMIC device.

18. The E-Band transceiver front-end according to Claim 17, further comprising a phase lock loop circuit comprising a X1/8 multiplier, a phase lock loop device downstream of said X1/8 multiplier, and a reference signal oscillator which supplies a reference signal to an input of said phase lock loop device, wherein an output of said phase lock loop device is in communication with an input of said fixed tune oscillator of said third MMIC device, and wherein said X1/8 multiplier is in communication with a second output of said third device power divider from said third MMIC device.

19. The E-Band transceiver front-end according to Claim 17, wherein said at least one transmission amplifier comprises a first and second transmission amplifier in series.

20. The E-Band transceiver front-end according to Claim 17, wherein said first, second, and third MMIC devices are manufactured by a p-HEMT process.

21. The E-Band transceiver front-end to Claim 17, wherein said first and second MMIC devices are manufactured by a p-HEMT process and said third MMIC device is manufactured by a MESFET process.

22. The E-Band transceiver front-end according to Claim 17, wherein said transceiver front-end transmits and receives over three frequency ranges including 71-76 GHz, 81-86 GHz and 92-95 GHz.

23. The E-Band transceiver front-end according to Claim 22, wherein said transceiver front-end transmits and receives over four 1.25 GHz channels within each of the 71-76 GHz , 81-86 GHz, and 92-95 frequency ranges.

24. The E-Band transceiver front-end according to Claim 17, wherein said MMIC devices are gallium arsenide (GaAs) devices.

25. The E-Band transceiver front-end according to Claim 17, wherein said transceiver front-end is adapted to communicate with another transceiver front-end in a full-duplex scheme.

26. A MMIC-based E-Band transceiver front-end comprising:

a first MMIC device comprising,

a transmission circuit comprising a sub-harmonic transmission mixer, at least one transmission amplifier downstream said transmission mixer, wherein a data steam is input into said transmission mixer, and wherein an output from said at least one amplifier is transmitted;

a receiver circuit comprising a low noise amplifier, a receiver bandpass filter downstream said low noise amplifier, and a sub-harmonic receiver mixer, wherein a received signal is communicated to an input of said low noise amplifier, and wherein an output of said receiver mixer is communicated to a third MMIC device; and

an LO signal circuit comprising a power divider, a transmission LO amplifier in communication with a first output of said power divider, and a receiver LO amplifier in communication with a second output of said power divider, wherein an output of said transmission LO amplifier is communicated to an input of said transmission mixer, and an output of said receiver LO amplifier is communicated to an input of said receiver mixer;

a second MMIC device comprising a multiplier circuit.comprising a multiplier circuit amplifier, a X4 multiplier downstream of said multiplier circuit amplifier, and a multiplier circuit bandpass filter downstream of said X4 multiplier, wherein an output of

said multiplier circuit bandpass filter is communicated to an input of said power divider of said first MMIC device; and

said third MMIC device comprising,

an IF circuit comprising an IF amplifier, a low pass filter downstream of said IF amplifier, and a baseband mixer downstream of said low pass filter, wherein an output of said receiver mixer from said first MMIC device is communicated to an input of said IF amplifier, and wherein said baseband mixer provides an output data stream; and

an LO generation circuit comprising a fixed tuned oscillator, a first buffering amplifier downstream of said fixed tuned oscillator, a coupler between said fixed tuned oscillator and said first buffering amplifier, a third MMIC device power divider downstream of said coupler, and a second buffering amplifier downstream of a first output of said third MMIC device power divider, wherein an output from said first buffering amplifier is communicated to an input of said multiplier circuit amplifier of said second MMIC device.

27. The E-Band transceiver front-end according to Claim 26, further comprising a phase lock loop circuit comprising a X1/8 multiplier, a phase lock loop device downstream of said X1/8 multiplier, and a reference signal oscillator which supplies a reference signal to an input of said phase lock loop device, wherein an output of said phase lock loop device is in communication with an input of said fixed tune oscillator of said third MMIC device, and wherein said X1/8 multiplier is in communication with a second output of said third MMIC device power divider .

28. The E-Band transceiver front-end according to Claim 26, wherein said at least one transmission amplifier comprises a first and second transmission amplifier in series.

29. The E-Band transceiver front-end according to Claim 26, wherein said first, second, and third MMIC devices are manufactured by a p-HEMT process.

30. The E-Band transceiver front-end to Claim 26, wherein said first and second MMIC devices are manufactured by a p-HEMT process and said third MMIC device is manufactured by a MESFET process.

31. The E-Band transceiver front-end according to Claim 26, wherein said transceiver front-end transmits and receives over three frequency ranges including 71-76 GHz, 81-86 GHz and 92-95 GHz.

32. The E-Band transceiver front-end according to Claim 31, wherein said transceiver front-end transmits and receives over four 1.25 GHz channels within each of the 71-76 GHz , 81-86 GHz, and 92-95 frequency ranges.

33. The E-Band transceiver front-end according to Claim 26, wherein said MMIC devices are gallium arsenide (GaAs) devices.

34. The E-Band transceiver front-end according to Claim 26 wherein said transceiver front-end is adapted to communicate with another transceiver front-end in a full-duplex scheme.

35. A MMIC-based E-Band transceiver front-end consisting:

a first MMIC device consisting,

a transmission circuit consisting of a sub-harmonic transmission mixer, and a transmission amplifier downstream said transmission mixer, wherein a data steam is input into said transmission mixer, and wherein an output from said at least one amplifier is transmitted;

a receiver circuit consisting of a low noise amplifier, a receiver bandpass filter downstream said low noise amplifier, and a sub-harmonic receiver mixer, wherein a received signal is communicated to an input of said low noise amplifier, and wherein an output of said receiver mixer is communicated to a second MMIC device; and

an LO signal circuit consisting of a power divider, a transmission LO amplifier in communication with a first output of said power divider, and a receiver LO amplifier in communication with a second output of said power divider, wherein an output of said transmission LO amplifier is communicated to an input of said transmission mixer, and an output of said receiver LO amplifier is communicated to an input of said receiver mixer; and

a second MMIC device consisting,

a multiplier circuit consisting of a first buffering amplifier, an X4 multiplier downstream of said first buffering amplifier, and a multiplier circuit bandpass filter downstream of said X4 multiplier, wherein an output of said multiplier circuit

bandpass filter is communicated to an input of said power divider of said first MMIC device;

an IF circuit consisting of an IF amplifier, a low pass filter downstream of said IF amplifier, and a baseband mixer downstream of said low pass filter, wherein an output of said receiver mixer from said first MMIC device is communicated to an input of said IF amplifier, and wherein said baseband mixer provides an output data stream; and

an LO generation circuit consisting of a fixed tuned oscillator having an output in communication with an input of said first buffering amplifier of said multiplier circuit, a coupler between said fixed tuned oscillator and said first buffering amplifier, a second MMIC device power divider downstream of said coupler, and a second buffering amplifier downstream of a first output of said second MMIC device power divider.

36. The E-Band transceiver front-end according to Claim 35, further comprising a phase lock loop circuit comprising a X1/8 multiplier, a phase lock loop device downstream of said X1/8 multiplier, and a reference signal oscillator which supplies a reference signal to an input of said phase lock loop device, wherein an output of said phase lock loop device is in communication with an input of said fixed tune oscillator of said third MMIC device, and wherein said X1/8 multiplier is in communication with a second output of said second MMIC device power divider.

37. The E-Band transceiver front-end according to Claim 35, wherein said first and second MMIC devices are manufactured by a p-HEMT process.

38. The E-Band transceiver front-end according to Claim 35, wherein said transceiver front-end transmits and receives over three frequency ranges including 71-76 GHz, 81-86 GHz and 92-95 GHz.

39. The E-Band transceiver front-end according to Claim 38, wherein said transceiver front-end transmits and receives over four 1.25 GHz channels within each of the 71-76 GHz , 81-86 GHz, and 92-95 frequency ranges.

40. The E-Band transceiver front-end according to Claim 35, wherein said MMIC devices are gallium arsenide (GaAs) devices.

41. The E-Band transceiver front-end according to Claim 35, wherein said transceiver front-end is adapted to communicate with another transceiver front-end in a full-duplex scheme.

42. A MMIC device comprising:

a transmission circuit comprising a fundamental transmission mixer, at least one transmission amplifier downstream said transmission mixer, wherein a data steam is input into said transmission mixer, and wherein an output from said at least one amplifier is transmitted;

a receiver circuit comprising a low noise amplifier, a receiver bandpass filter downstream said low noise amplifier, and a fundamental receiver mixer, wherein a received signal is communicated to an input of said low noise amplifier; and

an LO signal circuit comprising a power divider, a transmission LO amplifier in communication with a first output of said power divider, and a receiver LO amplifier in communication with a second output of said power divider, wherein an output of said transmission LO amplifier is communicated to an input of said transmission mixer, and an output of said receiver LO amplifier is communicated to an input of said receiver mixer.

43. A MMIC device comprising:

a multiplier circuit comprising an X2 multiplier, a first multiplier circuit bandpass filter downstream of said X2 multiplier, a multiplier circuit amplifier downstream of said first multiplier circuit bandpass filter, a X4 multiplier downstream of multiplier circuit amplifier, and a second multiplier circuit bandpass filter downstream of said X4 multiplier.

44. A MMIC device comprising:

an IF circuit comprising an IF amplifier, a low pass filter downstream of said IF amplifier, and a baseband mixer downstream of said low pass filter, wherein an output of said receiver mixer from said first MMIC device is communicated to an input of said IF amplifier, and wherein said baseband mixer provides an output data stream; and

an LO generation circuit comprising a fixed tuned oscillator, a first buffering amplifier downstream of said fixed tuned oscillator, a coupler between said

fixed tuned oscillator and said first buffering amplifier, a third MMIC device power divider downstream of said coupler, and a second buffering amplifier downstream of a first output of said third MMIC device power divider.

45. A MMIC device comprising:

a transmission circuit comprising a sub-harmonic transmission mixer, at least one transmission amplifier downstream said transmission mixer, wherein a data steam is input into said transmission mixer, and wherein an output from said at least one amplifier is transmitted;

a receiver circuit comprising a low noise amplifier, a receiver bandpass filter downstream said low noise amplifier, and a sub-harmonic receiver mixer, wherein a received signal is communicated to an input of said low noise amplifier; and

an LO signal circuit comprising a power divider, a transmission LO amplifier in communication with a first output of said power divider, and a receiver LO amplifier in communication with a second output of said power divider, wherein an output of said transmission LO amplifier is communicated to an input of said transmission mixer, and an output of said receiver LO amplifier is communicated to an input of said receiver mixer.

46. A MMIC device comprising:

a multiplier circuit comprising a first buffering amplifier, an X4 multiplier downstream of said first buffering amplifier, and a multiplier circuit bandpass filter downstream of said X4 multiplier;

an IF circuit comprising an IF amplifier, a low pass filter downstream of said IF amplifier, and a baseband mixer downstream of said low pass filter, wherein an output of said receiver mixer from said first MMIC device is communicated to an input of said IF amplifier, and wherein said baseband mixer provides an output data stream; and

an LO generation circuit comprising a fixed tuned oscillator having an output in communication with an input of said first buffering amplifier of said multiplier circuit, a coupler between said fixed tuned oscillator and said first buffering amplifier, a second MMIC device power divider downstream of said coupler, and a second buffering amplifier downstream of a first output of said second MMIC device power divider.

47. An E-Band communications system comprising a plurality of E-Band stations adapted to communicate with each other, each station comprising a MMIC-based E-Band transceiver front-end, a modem, baseband equipment, and a data source, said MMIC-based E-Band transceiver front-end comprising:

a first MMIC device comprising,

a transmission circuit for receiving a data stream input at a baseband frequency, mixing the data stream with an LO signal having an E-Band frequency, and transmitting a resultant data stream at an upconverted E-Band frequency;

a receiver circuit for receiving a data stream having an E-Band frequency, mixing the received data stream with an LO signal having an E-Band frequency, and downconverting the resultant mixed received signal to an intermediate frequency (IF); and

an LO signal circuit for dividing a received LO signal at an E-Band frequency and communicating the LO signal to said transmission and receiver circuits;

a second MMIC device comprising a multiplier circuit for receiving an LO signal at a reference frequency, and multiplying the LO signal to an E-Band frequency;

a third MMIC device comprising,

a second downconversion circuit for mixing the mixed received IF signal with an LO signal, and downconverting the resultant mixed received signal to a baseband frequency, and

an LO generation circuit for generating an LO signal, communicating the LO signal to said second MMIC device, coupling the LO signal, dividing the coupled LO signal, and communicating the divided LO signal to the second downconversion circuit.

48. The E-Band communications system according to Claim 47, wherein said first, second, and third MMIC devices are manufactured by a p-HEMT process.

49. The E-Band communications system according to Claim 47, wherein said first and second MMIC devices are manufactured by a p-HEMT process and said third MMIC device is manufactured by a MESFET process.

50. The E-Band communications system according to Claim 47, wherein said transceiver front-end transmits and receives over three frequency ranges including 71-76 GHz, 81-86 GHz and 92-95 GHz.

51. The E-Band communications system according to Claim 48, wherein said transceiver front-end transmits and receives over four 1.25 GHz channels within each of the 71-76 GHz , 81-86 GHz, and 92-95 frequency ranges.

52. The E-Band communications system according to Claim 47, wherein said MMIC devices are gallium arsenide (GaAs) devices.

53. The E-Band communications system according to Claim 47, wherein said transceiver front-end is adapted to communicate with another transceiver front-end in a full-duplex scheme.

54. The E-Band communications system according to Claim 47, wherein said transmission circuit includes a fundamental mixer and at least one amplifier downstream of said mixer.

55. The E-Band communications system according to Claim 47, wherein said receiving circuit includes a low noise amplifier, a bandpass filter downstream said low noise amplifier, and a fundamental mixer downstream said low noise amplifier.

56. The E-Band communications system according to Claim 47, wherein said LO signal circuit comprises a power divider and at least one amplifier downstream each output of said divider.

57. The E-Band communications system according to Claim 47, wherein said multiplier circuit comprises an X2 multiplier, a first bandpass filter downstream said X2 multiplier, a circuit amplifier downstream said first bandpass filter, a X4 multiplier downstream of said multiplier circuit amplifier, and a multiplier circuit bandpass filter downstream of said X4 multiplier.

58. The E-Band communications system according to Claim 47, said second downconversion circuit comprises at least one amplifier, a low pass filter downstream of said at least one amplifier, and a mixer downstream of said low pass filter.

59. The E-Band communications system according to Claim 48, wherein said LO generation circuit comprises an oscillator, at least one buffering amplifier downstream said oscillator, a coupler between said oscillator and said at least one buffering amplifier, a power divider downstream of said coupler, and a second amplifier downstream an output of said power divider.

60. The E-Band communications system according to Claim 47, wherein a sub-harmonic mixing scheme is utilized.

61. The E-Band communications system according to Claim 60, said wherein said transmission circuit and said receiver circuit each utilize singly balanced sub-harmonic mixers.

62. The E-Band communications system according to Claim 61, wherein said multiplier circuit comprises a circuit amplifier, a X4 multiplier downstream of said multiplier circuit amplifier, and a multiplier circuit bandpass filter downstream of said X4 multiplier.

63. The E-Band communications system according to Claim 47, wherein said system implements a point-to-point topology.